WHAT IS CLAIMED IS:

1. A method of fabricating an interconnect structure, comprising:

providing a semiconductor substrate having a first conductive layer thereon;

forming a dielectric layer overlying the semiconductor substrate and the first conductive layer;

forming an opening in the dielectric layer extending to the first conductive layer;

removing a portion of the first conductive layer through the opening to form a recess having a substantially curvilinear profile; and

filling the opening and the recess with a second conductive layer.

2. The method of claim 1 wherein the recess has a depth of at least 200 Å.

3. The method of claim 1 wherein the recess has a depth ranging between about 300 Å and about 800 Å.

4. The method of claim 1 wherein the recess has a depth ranging between about 500 Å and about 700 Å.

5. The method of claim 1 wherein removing a portion of the first conductive layer comprises sputtering.

6. The method of claim 1 wherein removing a portion of the first conductive layer comprises sputtering employing a self-ionized plasma (SIP) system.

7. The method of claim 1 wherein removing a portion of the first conductive layer comprises sputtering employing an ionized metal plasma (IMP) system.

8. The method of claim 1 further comprising forming a diffusion barrier layer lining the sidewalls of the opening prior to removing a portion of the first conductive layer.

9. The method of claim 1 further comprising forming a diffusion barrier layer conformal to the profile of the recess before filling the opening and the recess.

10. The method of claim 1 wherein the recess profile is substantially W-shaped.

11. The method of claim 1 wherein the recess profile includes a peak having a height ranging between about 25% and about 75% of a depth of the recess.

12. The method of claim 1 wherein the recess profile includes a peak having a height that is about 50% of a depth of the recess.

13. The method of claim 1 wherein the recess profile is substantially concave.

14. The method of claim 1 wherein the recess profile is a shallow-peaked profile including a peak having a height ranging between about 5% and about 25% of a depth of the recess.

15. The method of claim 1 wherein the recess profile is a substantially trapezoidal, peaked profile.

16. A method of fabricating an interconnect structure, comprising:

providing a semiconductor substrate having a first conductive layer thereon;

forming a dielectric layer overlying the semiconductor substrate and the first conductive layer;

forming an opening in the dielectric layer exposing the first conductive layer;

forming a diffusion barrier layer at least partially lining the opening by employing one of a self-ionized plasma (SIP) system and an ionized metal plasma (IMP) system;

removing a portion of the first conductive layer in-situ through the opening to form a recess having a substantially curvilinear profile in the first conductive layer by employing one of the SIP system and the IMP system; and

filling the opening and the recess with a second conductive layer.

17. The method of claim 16 wherein the recess has a depth of at least 200 Å.

18. The method of claim 16 wherein the recess has a depth ranging between about 300 Å and about 800 Å.

19. The method of claim 16 wherein the recess has a depth ranging between about 500 Å and about 700 Å.

20. The method of claim 16 further comprising forming a diffusion barrier layer substantially conformal to the profile of the recess before filling the opening and the recess.

21. The method of claim 16 wherein the recess profile is substantially W-shaped.

22. The method of claim 16 wherein the recess profile includes a peak having a height ranging between about 25% and about 75% of a depth of the recess.

23. The method of claim 16 wherein the recess profile includes a peak having a height that is about 50% of a depth of the recess.

24. The method of claim 16 wherein the recess profile is substantially concave.

25. The method of claim 16 wherein the recess profile is a shallow-peaked profile including a peak having a height ranging between about 5% and about 25% of a depth of the recess.

26. The method of claim 16 wherein the recess profile is a substantially trapezoidal, peaked profile.

27. An interconnect structure, comprising:

a first conductive layer located in a substrate;

a dielectric layer overlying the first conductive layer and having an opening extending to the first conductive layer; and

a second conductive layer located in the opening and contacting a portion of the first conductive layer, wherein an interface between the first and second conductive layers substantially conforms to a substantially curvilinear profile.

28. The interconnect structure of claim 27 wherein the profile has a depth relative to the substrate of at least 200 Å.

29. The interconnect structure of claim 27 wherein the profile has a depth relative to the substrate ranging between about 300 Å and about 800 Å.

30. The interconnect structure of claim 27 wherein the profile has a depth relative to the substrate ranging between about 500 Å and about 700 Å.

31. The interconnect structure of claim 27 further comprising a diffusion barrier layer interposing the dielectric layer and the second conductive layer.

32. The interconnect structure of claim 27 further comprising a diffusion barrier layer interposing the first and second conductive layers and substantially conforming to the interface profile.

33. The interconnect structure of claim 27 wherein the interface profile is substantially W-shaped.

34. The interconnect structure of claim 27 wherein the interface profile includes a peak having a height ranging between about 25% and about 75% of a depth of the interface profile relative to the substrate.

35. The interconnect structure of claim 27 wherein the interface profile includes a peak having a height that is about 50% of a depth of the interface profile relative to the substrate.

36. The interconnect structure of claim 27 wherein the interface profile is substantially concave relative to the substrate.

37. The interconnect structure of claim 27 wherein the interface profile is a shallow-peaked profile including a peak having a height ranging between about 5% and about 25% of a depth of the interface profile relative to the substrate.

38. The interconnect structure of claim 27 wherein the interface profile is a substantially trapezoidal, peaked profile.

39. The interconnect structure of claim 27 wherein the opening is one of a via hole opening and a dual damascene opening.

40. The interconnect structure of claim 27 wherein at least one of the first and second conductive layers comprises one of copper and a copper alloy.

41. An integrated circuit device, comprising:

a plurality of semiconductor devices coupled to a substrate; and

an interconnect structure coupling ones of the plurality of semiconductor devices, the interconnect structure including:

a plurality of first conductive layers;

a dielectric layer overlying ones of the plurality of first conductive layers and having a plurality of openings each extending to one of the plurality of first conductive layers; and

a plurality of second conductive layers located in ones of the plurality of openings and each contacting a portion of one of the plurality of first conductive layers, wherein each interface between corresponding ones of the first and second conductive layers substantially conforms to a substantially curvilinear profile.

42. The integrated circuit device of claim 41 wherein the profile has a depth relative to a corresponding one of the plurality of first conductors of at least 200 Å.

43. The integrated circuit device of claim 41 wherein the profile has a depth relative to a corresponding one of the plurality of first conductors ranging between about 300 Å and about 800 Å.

44. The integrated circuit device of claim 41 wherein the profile has a depth relative to a corresponding one of the plurality of first conductors ranging between about 500 Å and about 700 Å.

45. The integrated circuit device of claim 41 wherein the interconnect structure further includes a plurality of diffusion barrier layers each interposing the dielectric layer and one of the plurality of second conductive layers.

46. The integrated circuit device of claim 41 wherein the interconnect structure further includes a plurality of diffusion barrier layers each interposing one of the plurality of first conductive layers and a corresponding one of the plurality of second conductive layers.

47. The integrated circuit device of claim 41 wherein the profile is substantially W-shaped.

48. The integrated circuit device of claim 41 wherein the profile includes a peak having a height ranging between about 25% and about 75% of a depth of the profile relative to a corresponding one of the plurality of first conductive layers.

49. The integrated circuit device of claim 41 wherein the profile is substantially concave relative to a corresponding one of the plurality of first conductive layers.

50. The integrated circuit device of claim 41 wherein the profile is a shallow-peaked profile including a peak having a height ranging between about 5% and about 25% of a depth of the profile relative to a corresponding one of the plurality of first conductive layers.

51. The integrated circuit device of claim 41 wherein the profile is a substantially trapezoidal, peaked profile.